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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,293	03/30/2001	James Wang	388682000600	6817

7590 09/09/2005

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EXAMINER	
MERED, HABTE	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,293	WANG ET AL	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 06 November 2002 requesting title change for the application has been entered.

Claim Objections

2. Claim 17 is objected to because of the following informalities: Claim 17 depends on a non-existing claim 18. The Examiner has examined claim 17 under the assumption that this claim depends on independent claim 15.. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ray et al (US 6, 631, 130), hereinafter referred to as Ray, in view of Hamlin et al (R.W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), hereinafter referred to as Hamlin.

Ray discloses a switching system that handles ATM, TDM, and packet data and in order to handle SONET frames it uses Path Overhead Processors.

5. Regarding **claim 1**, Ray discloses in a digital optical network, a method of buffering and reading path overhead bytes **(Applicant admits that this is being done**

in prior art as clearly stated on Page 5, Lines 12-15), comprising: identifying a plurality of path overhead bytes as they are received **(Figure 1A, element 18 is a POH Processor. See also Column 5: Lines 25-30 and Column 10, Lines 54-64);** determining a signal number (S#) for each of the path overhead bytes **(The SPE ID in Ray's system is the signal number and is four bits long like the Applicants as shown in Figure 6 of the drawings of the Applicant. See also Column 10, Lines 58-62)**.

Ray however fails to expressly to disclose how the POH processor works in storing the Path Overhead bytes and any associated information.

Hamlin discloses a SONET/SDH Overhead Terminator to process TOH and POH bytes independently and buffer them in a RAM.

Hamlin discloses a method of determining a path overhead number (P#) for each of the path overhead bytes; storing the path overhead bytes, signal numbers (S#), and path overhead numbers (P#) into a RAM FIFO buffer, wherein the RAM FIFO comprises a plurality of entries, each entry comprising a first section for storing a path overhead byte, a second section for storing a signal number (S#), and a third section for storing a path overhead number (P#); and reading the entries from the RAM FIFO, wherein the entries are stored and read from the RAM FIFO in accordance with a first-in-first-out (FIFO) protocol. **(Hamlin in Figure 2 shows an entity for de-multiplexing the TOH and POH from the received SONET signal and storing each item in a RAM. The RAM FIFO is shown in Figure 3 and further illustrated on Page 277, Section III, 2nd Paragraph. Hamlin further**

shows that the POH and the TOH are separately entered in different registered write ports in the RAM. The POH number can be any number the designer may choose including the address it is stored at. Clearly Hamlin teaches that POH can be stored in a RAM one byte at a time and given Ray's teaching of identifying Signals, it is strictly a design issue to determine what items are stored where as the combination of Ray and Hamlin teaches how to identify the items and where and how to store the items in question.)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ray's method to incorporate a method to process POH byte that includes storing it in a buffer. The motivation is that Ray discloses the need to process Path Overhead (POH) in Column 11, Lines 2-3. Hamlin shows why overhead bytes like POH are continuously accessed and shows how it is processed in the last two paragraphs in Column 1 on Page 276.

6. Regarding **claim 6**, Ray discloses a method wherein the step of storing comprises storing only path overhead bytes meeting desired criteria, wherein the desired criteria includes any combination of the signal numbers (S#) and the path overhead numbers (P#). **(See Column 10, Lines 58-62; The criteria that determines which POH is stored is a design issue driven by a specific task and since Ray teaches how to identify the POH and the signal it is straight forward for one skilled in the art to come up with such a criteria if the task to accomplish is determined).**

7. **Claims 2–5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ray in view of Hamlin as applied to claim 1 above, and further in view of Noeldner et al (US 6, 449, 666), hereinafter referred to as Noeldner.

8. Regarding **Claim 2**, the combination of Ray and Hamlin teaches all aspects of the claimed invention as set forth in the rejections of claim 1 but does not disclose a method further comprising: incrementing a first counter each time one of the path overhead bytes is stored in one of the entries; incrementing a second counter for each entry that is read; determining when a difference in values between the first counter and the second counter reaches a specified value (N); generating an interrupt signal when the difference reaches N; transmitting the interrupt signal to a processor; and initiating the step of reading when the interrupt signal is received by the processor.

Noeldner teaches an optimized data controller coupled to a RAM as shown in Figure 1.

Noeldner discloses a method of incrementing a first counter each time one of the path overhead bytes is stored in one of the entries **(In Noeldner's system a Tail Pointer register is incremented when data is written in the RAM and space is removed from the free pointer list (i.e. a free pointer is removed). See Column 7, Lines 15-26)**; incrementing a second counter for each entry that is read **(In Noeldner's system a Head Pointer register is incremented when data is read out from the RAM and space is added to the free pointer list (i.e. a free pointer is added). See Column 7, Lines 15-26)**; determining when a difference in values between the first counter and the second counter reaches a specified value (N) **(See Column 7, Lines**

28-30; In Noeldner's system comparison is done to see when the RAM is full which is equivalent to when the free pointer list is empty. Further the head and tail pointer registers automatically wrap to zero to prevent overflow. Of course in Column 7, Lines 30-35 Noeldner shows that a difference can be added so the difference in the registers comparison will not be zero to accomplish any range of design goals.); generating an interrupt signal when the difference reaches **N (N being zero in Noeldner case an interrupt is not necessary but the system has ability to generate interrupts based on whether a queue is empty or full; See Column 28, Lines 50-67)**; transmitting the interrupt signal to a processor; and initiating the step of reading when the interrupt signal is received by the processor **(See Column 28, Lines 50-67; When an interrupt occurs the processor will take step to either discard the incoming data or remove the stored data and either choice is strictly a design issue dependent on the task to be accomplished.)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of when data is written into the buffer and read out from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

9. Regarding **claim 3**, the combination of Ray and Hamlin teaches all aspects of the claimed invention as set forth in the rejections of claim 1 but does not disclose a

method further comprising: incrementing a first counter each time one of the path overhead bytes is stored in one of the entries; incrementing a second counter for each entry that is read; periodically polling the first and second counters at specified time intervals to determine a difference in values between the first and second counters; and initiating the step of reading when the difference reaches a specified value.

Noeldner discloses a method further comprising: incrementing a first counter each time one of the path overhead bytes is stored in one of the entries **(Tail Pointer register is incremented. See Column 7, Lines 15-26);** incrementing a second counter for each entry that is read **(Head Pointer register is incremented. See Column 7, Lines 15-26)**; periodically polling the first and second counters at specified time intervals to determine a difference in values between the first and second counters **(Noeldner's system does polling of different registers as indicated in Column 6, Lines 7-11; Further in Noeldner's system these registers in question wrap to zero and overflow will not occur. As a design choice the incoming data gets discarded rather than forcing the removal of the stored data. However some form of polling or monitoring of these registers is done to determine when the buffer is full as shown in Column 7, Lines 28-35)**; and initiating the step of reading when the difference reaches a specified value **(Strictly a design issue as the incoming data can be discarded instead as is the case with Noeldner)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of

when data is written into the buffer and read out from the buffer and polling these registers. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

10. Regarding **claim 4**, the combination of Ray and Hamlin teaches all aspects of the claimed invention as set forth in the rejections of claim 1 but does not disclose a method wherein the step of reading comprises burst mode reading of entries from the RAM FIFO.

Noeldner discloses a method wherein the step of reading comprises burst mode reading of entries from the RAM FIFO. **(See Column 26, Line 19)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of when data is written into the buffer and read out in *burst* form from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

11. Regarding **claim 5**, the combination of Ray and Hamlin teaches all aspects of the claimed invention as set forth in the rejections of claim 1 but does not disclose a

method wherein the step of reading comprises direct memory access (DMA) reading of entries from the RAM FIFO.

Noeldner discloses a method wherein the step of reading comprises direct memory access (DMA) reading of entries from the RAM FIFO. **(See Figure 2, element 225)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of when data is written into the buffer and *DMA* read from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

12. **Claims 7, 15 and16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ray et al (US 6, 631, 130), hereinafter referred to as Ray, in view of Hamlin et al (R.W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), hereinafter referred to as Hamlin, and Jennings (US 5, 559, 969).

13. Regarding **claim 7 and 15**, Ray discloses a digital optical network, a method and apparatus of buffering and reading path overhead bytes **(Applicant admits that this is being done in prior art as clearly stated on Page 5, Lines 12-15)**, comprising: identifying a plurality of path overhead bytes as they are received **(Figure 1A, element 18 is a POH Processor. See also Column 5: Lines 25-30 and Column 10, Lines 54-64)**; determining a signal number (S#) for each of the path overhead bytes **(The SPE ID**

in Ray's system is the signal number and is four bits long like the Applicants as shown in Figure 6 of the drawings of the Applicant. See also Column 10, Lines 58-62).

Ray however fails to expressly to disclose how the POH processor works in storing the Path Overhead bytes and any associated information.

Hamlin discloses determining a path overhead number (P#) for each of the path overhead bytes; storing the path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a first RAM FIFO buffer, wherein the RAM FIFO includes a plurality of entries, each entry comprising a first section for storing a respective path overhead byte, a second section for storing a respective signal number (S#), and a third section for storing a respective path overhead number (P#). **(Hamlin in Figure 2 shows an entity for de-multiplexing the TOH and POH from the received SONET signal and storing each item in a RAM. The RAM FIFO is shown in Figure 3 and further illustrated on Page 277, Section III, 2nd Paragraph. Hamlin further shows that the POH and the TOH are separately entered in different registered write ports in the RAM. The POH number can be any number the designer may choose including the address it is stored at. Clearly Hamlin teaches that POH can be stored in a RAM one byte at a time and given Ray's teaching of identifying Signals, it is strictly a design issue to determine what items are stored where as the combination of Ray and Hamlin teaches how to identify the items and where and how to store the items in question.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ray's method to incorporate a POH byte that includes storing it in a buffer. The motivation is that Ray discloses the need to process Path Overhead (POH) in Column 11, Lines 2-3. Hamlin shows why overhead bytes like POH are continuously accessed and shows how it is processed in the last two paragraphs in Column 1 on Page 276.

Ray fails to expressly disclose that different subset of the overhead bytes, signal numbers, and path overhead numbers can be stored in two different RAM buffers.

Jennings discloses a method for effectively interfacing variable width data streams to a fixed width memory.

Jennings discloses storing a first subset of the path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a first RAM FIFO buffer, wherein the first RAM FIFO includes a plurality of entries, each entry comprising a first section for storing a respective path overhead byte, a second section for storing at least a portion of a respective signal number (S#), and a third section for storing a respective path overhead number (P#), wherein the first subset of path overhead bytes have signal numbers corresponding to a first set of values; storing a second subset of the path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a second RAM FIFO buffer, wherein the second RAM FIFO includes a plurality of entries, each entry comprising a first section for storing a respective path overhead byte, a second section for storing at least a portion of a respective signal number (S#), and a third section for storing a respective path overhead number (P#), wherein the second

subset of path overhead bytes have signal numbers corresponding to a second set of values; and reading the entries from the first and second RAM FIFO, wherein entries are stored and read from each respective first and second RAM FIFO in accordance with a first-in-first-out (FIFO) protocol. **(Applicant describes these limitations as the solution to a problem described on Page 13, Lines 18-20. The problem the Applicant is addressing is how to use the bandwidth of a data bus efficiently without being forced to send data in two cycles of 16-bit wide bus when using a 32-bit bus. This is an age old problem in data design in that the designer in a shared data bus has to maximize use of the data bus in that in this case has to use all 32 bits and the choices are either sending it in two cycles of 16-bit wide data or else re-format the data and send it in one cycle like the Applicant did. Jennings describes the problem of the criticality of the efficient use of a shared data bus in Column 2, Lines 44-55. Jennings like the Applicant shows a general possible solution is to reformat the data so that it can be read in one cycle in Column 3, Lines 50-60. The Applicant when processing 48 STS signal it is obvious it has to use 4 RAM FIFO buffers but in order to send the data it reformats it and sends in one cycle. However in this process as far as the Examiner can determine each RAM stores a group of POH belonging to a group of known signals but the ability to associate each POH with each signal is now lost. As far as using two RAM buffers to store overhead data is admitted as a prior art by the Applicant on Page 5, Line 15.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ray's method to send data in one cycle over a shared bus. The motivation is that in Ray's system as shown in Figure 1 there are a multitude of shared buses. Jennings discloses the importance of using efficiently a bus shared by high processors like that of Roy's SONET framers or POH processors and slow processors like memory access systems as indicated in Column 2, Lines 25-35.

14. Regarding **claim 16**, Ray discloses all aspects of the claimed invention as set forth in the rejection of claim 15 but fails to disclose each entry of the first and second plurality of entries comprises sixteen bits of storage capacity, each of the first sections comprises eight bits of storage capacity, each of the second sections comprises four bits of storage capacity, and each of the third sections comprises four bits of storage capacity.

Hamlin discloses each entry of the first and second plurality of entries comprises sixteen bits of storage capacity, each of the first sections comprises eight bits of storage capacity, each of the second sections comprises four bits of storage capacity, and each of the third sections comprises four bits of storage capacity. **(Hamlin discloses a RAM FIFO buffer to store POH. There is no reason to assume the capacity indicated by the limitation cannot be met by Hamlin's system. The RAM FIFO is shown in Figure 3 and further illustrated on Page 277, Section III, 2nd Paragraph. Hamlin further shows that the POH and the TOH are separately entered in different registered write ports in the RAM.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ray's method to incorporate a method to process POH byte that includes storing it in a buffer. The motivation is that Ray discloses the need to process Path Overhead (POH) in Column 11, Lines 2-3. Hamlin shows why overhead bytes like POH are continuously accessed and shows how it is processed in the last two paragraphs in Column 1 on Page 276.

15. **Claims 8–11 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ray in view of Hamlin and Jennings as applied to claim 7 above, and further in view of Noeldner et al (US 6, 449, 666), hereinafter referred to as Noeldner.

16. Regarding **claims 8 and 9**, the combination of Ray and Hamlin and Jennings teaches all aspects of the claimed invention as set forth in the rejections of claim 7 but does not disclose a method wherein the step of reading comprises burst mode reading of entries from the RAM FIFO.

Noeldner discloses a method wherein the step of reading comprises burst mode reading of entries from the RAM FIFO. **(See Column 26, Line 19)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of when data is written into the buffer and read out in *burst* form from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-

17. Regarding **claim 10**, the combination of Ray and Hamlin and Jennings teaches all aspects of the claimed invention as set forth in the rejections of claim 7 but does not disclose wherein the step of reading comprises direct memory access (DMA) reading the first and second RAM FIFOs in parallel.

Noeldner discloses a method wherein the step of reading comprises direct memory access (DMA) reading of entries from the RAM FIFO. **(See Figure 2, element 225)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of when data is written into the buffer and *DMA* read from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

18. Regarding **claim 11**, Ray discloses a method wherein the steps of storing comprise storing only path overhead bytes meeting desired criteria into the respective first and second RAM FIFOs, wherein the desired criteria includes any combination of the signal numbers (S#) and the path overhead numbers (P#). **(See Column 10, Lines 58-62; The criteria that determines which POH is stored is a design issue driven by a specific task and since Ray teaches how to identify the POH and the signal it is straight forward for one skilled in the art to come up with such a criteria if the task to accomplish is determined).**

19. Regarding **claim 17**, the combination of Ray and Hamlin and Jennings teaches all aspects of the claimed invention as set forth in the rejections of claim 15 but does not disclose an apparatus further comprising: a first counter that is incremented each time data an entry is stored in one of the first and second RAM FIFOs; and a second counter that is incremented for each entry that is read from the first and second RAM FIFOs.

Noeldner discloses an apparatus further comprising: a first counter that is incremented each time data an entry is stored in one of the first and second RAM FIFOs **(In Noeldner's system a Head Pointer register is incremented when data is read out from the RAM and space is added to the free pointer list (i.e. a free pointer is added). See Column 7, Lines 15-26)**; and a second counter that is incremented for each entry that is read from the first and second RAM FIFOs **(In Noeldner's system a Head Pointer register is incremented when data is read out from the RAM and space is added to the free pointer list (i.e. a free pointer is added). See Column 7, Lines 15-26)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of when data is written into the buffer and read out from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

20. **Claims 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin et al (R.W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), hereinafter referred to as Hamlin, in view of Ray et al (US 6, 631, 130), hereinafter referred to as Ray, in view of Hamlin et al.

21. Regarding **claim 12**, Hamlin discloses an apparatus for buffering path overhead bytes, comprising a RAM FIFO buffer having a plurality of entries, each entry comprising a first section for storing a path overhead byte and a second section for storing a path overhead number (P#). **(The RAM FIFO is shown in Figure 3 and further illustrated on Page 277, Section III, 2nd Paragraph. Hamlin further shows that the POH and the TOH are separately entered in different registered write ports in the RAM. The POH number can be any number the designer may choose including the address it is stored at. Any other information can be stored to uniquely identify the POH)**

Hamlin fails to disclose a signal number.

Ray discloses a signal number during the processing of Path Overhead bytes. **(The SPE ID in Ray's system is the signal number and is four bits long like the Applicants as shown in Figure 6 of the drawings of the Applicant. See also Column 10, Lines 58-62).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Hamlin's method to incorporate a method to identify signal number when processing POH bytes. The motivation is that Hamlin shows why overhead bytes like POH are continuously accessed and shows how it is processed in

the last two paragraphs in Column 1 on Page 276. Ray discloses the need to process Path Overhead (POH) in Column 11, Lines 2-3 which includes identifying the signal number.

22. Regarding **claim 13**, Hamlin discloses an apparatus wherein each entry of the plurality of entries comprises sixteen bits of storage capacity, the first section comprises eight bits of storage capacity, the second section comprises four bits of storage capacity, and the third section comprises four bits of storage capacity. **(Hamlin's RAM FIFO can handle the capacity mentioned in the limitation. The RAM FIFO is shown in Figure 3 and further illustrated on Page 277, Section III, 2nd Paragraph)**

23. **Claims 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamlin in view of Ray as applied to claim 12 above, and further in view of Noeldner et al (US 6, 449, 666), hereinafter referred to as Noeldner.

The combination of Hamlin and Ray teaches all aspects of the claimed invention as set forth in the rejections of claim 12 but does not disclose an apparatus further comprising: a first counter that is incremented each time one of the path overhead bytes is stored in one of the entries **(Tail Pointer register is incremented. See Column 7, Lines 15-26)**; and a second counter that is incremented for each of the entries that is read from the RAM FIFO **(Head Pointer register is incremented. See Column 7, Lines 15-26)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Ray's and Hamlin's apparatus with a mechanism for the Data Controller of the RAM involving registers keeping track of

when data is written into the buffer and read out from the buffer. The motivation is that Hamlin discloses a memory access mechanism that involves a RAM Controller. Noeldner discloses how a RAM Controller works in Column 1, Lines 33-43 and further discloses the need for an optimized RAM Controller in Column 2, Lines 20-25.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following US Patents also disclose similar subject matter:

US Patent (6, 580, 731) to Denton

US Patent (5, 331, 641) to Parruck et al

US Patent (5, 257, 261) to Parruck et al

US Patent (6, 502, 197) to Raza

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
09-02-2005

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600